Image Sensor with Correlated Double Sampling Technique using Switched-Capacitor Technology

This application claims the benefit of US Provisional Patent Application Serial No. 60/256,491 filed on December 20, 2000.

Field of the Invention

The invention relates generally to image scanning devices and more particularly to CMOS image sensors.

Background of the Invention

As telecommunication devices and personal digital assistants increase in popularity so do their demand for new and interesting features. Such features, which may include digital video communication or imbedded image capture apparatus, will require the use of a transducer with specifications compatible with the devices in question i.e. low power consumption, reduced size, high resolution, high speed.

Charged coupled devices (CCD) of the type disclosed in US 3,715,485 that issued to Weimer on February 6, 1973, are presently the most significant commercial IC transducer used to represent an image as an electrical signal. Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS) image sensors and CCD sensors were developed around the same time, however it was found when they were initially created, that CMOS image sensors had too poor a signal to noise ratio to be competitive. An elementary example of a CMOS imager is described in US 4,155,094 which issued to Ohba et al on May 15, 1979.

However, the CMOS sensor does have certain advantages over the CCD sensor. The CMOS image sensor has the ability to integrate companion circuitry such as digital signal processing circuitry onto the same substrate as the image sensor, allowing the reduction in size of the amount of peripheral circuitry needed to interface with the image sensor. Further, integrating processing and acquisition circuitry allows designers to take

advantage of a wider data-path between these stages.

As well, CMOS image sensors can be manufactured using current standard CMOS fabrication techniques, giving it a significant cost advantage over using the alternative CCD image sensor which requires special manufacturing techniques. CMOS is a less expensive technology employing fewer mask layers and is a more mature fabrication technology with greater commercial volume. CCD technology complexity causes lower fabrication yield.

The noise disadvantage of CMOS imagers has been addressed at various stages in the device; in particular there was the development of correlated double sampling (CDS), which is described in US 3,949,162 that issued to Malueg on April 6, 1976.

CDS is used when reading out information from the image pixels. This operation is performed by first reading out the level of the charge stored on the pixel element and storing it on a capacitor, and then by reading out the charge stored on the pixel element by a reset voltage and storing it on a capacitor. These two signals are then combined to form a noise-reduced signal representative of the pixel signal. This process reduces most of the noise associated with an active pixel sensor (APS), such as dark current noise, kT/C noise from the floating diffusion node, the fixed pattern noise (FPN) from the MOS transistor threshold voltage differences inside the pixel, and the low-frequency noise generated by the source-follower MOS transistors. However, this process does not reduce the column-wise FPN contributed by capacitor mismatching in the column readout circuitry.

Therefore, there is a need for a process and apparatus that effectively eliminates the fixed pattern noise contributed by the column readout circuitry.

Summary of the Invention

The invention is directed to a method and apparatus for processing an output signal of an image sensor pixel.

The method comprises applying a reference voltage V_{REF} to first and second capacitor elements that are coupled together at a common terminal, applying a first sample signal V_{S1} from the image sensor pixel to the first capacitor element placing a charge on it, transferring the charge from the first capacitor element to the second capacitor element, applying a second sample signal V_{S2} from the image sensor pixel to the first capacitor element placing a charge on it, and transferring the charge from the second capacitor element to the first capacitor element so as to provide an output signal that is a function of the difference between the second sample signal V_{S2} and the first sample signal V_{S1}.

In accordance with another aspect of this invention, an operational amplifier is coupled to the common terminal between the first and second capacitor elements, and the output of the operational amplifier is $V_O = V_{S2} - V_{S1} + V_{REF}$. In addition, V_{S1} is a sample voltage proportional to light intensity on the pixel and V_{S2} is a pixel reset voltage.

With regard to a further aspect of the present invention, the readout circuitry for image sensor pixels comprises a first capacitor element having first and second terminals, a second capacitor element having first and second terminals, an amplifier having an input terminal and an output terminal with the input terminal connected to the second terminals of the first and second capacitor elements. The readout circuitry further includes a first switch adapted to be connected between a reference voltage and the first terminal of the first capacitor element, a second switch adapted to be connected between a pixel and the first terminal of the first capacitor element, a third switch adapted to be connected between a reference voltage and the first terminal of the second capacitor element, a fourth switch connected between the amplifier input terminal and the output terminal, a fifth switch connected between the second terminal of the second capacitor element and the amplifier output terminal, and a sixth switch connected between the first terminal of the first capacitor element and the amplifier output terminal.

Regarding a further aspect of this invention, the readout circuitry further includes a controller for controlling the first to sixth switches. In particular the controller is adapted to close the first switch, the third switch and the fourth switch simultaneously, to close the second switch and the fifth switch simultaneously, to close the second switch and the fourth switch simultaneously, and then to close the third switch and the sixth switch simultaneously.

In accordance with a specific aspect of this invention, the amplifier is a CMOS operational amplifier with a reference terminal for connection to a reference voltage and all of the switches are CMOS transistors.

In accordance with another aspect of this invention, the method of operating the readout circuit outlined above comprises the following sequential steps: opening all of the switches, closing the first, third and fourth switches, opening all of the switches, closing the second and fifth switches, opening the fifth switch and closing the fourth switch, opening all of the switches, closing the third and sixth switches, and reading the output voltage Vo on the operational amplifier output terminal.

With the reference voltages being equal to V_{REF}, and the pixel sample signals being V_{S1} and V_{S2}, then $V_O = V_{S2} - V_{S1} + V_{REF}$. With V_{S1} being a sample voltage proportional to light intensity on the pixel and V_{S2} being a pixel reset voltage, the output Vo is a function of the light intensity on the pixel with no reliance on the values of the first and second capacitor elements.

Aspects and advantages of the invention, as well as the structure and operation of various embodiments of the invention, will become apparent to those ordinarily skilled in the art upon review of the following description of the invention in conjunction with the accompanying drawings.

Brief Description of the Drawings

The invention will be described with reference to the accompanying drawings, wherein:

Figure 1 illustrates a basic prior art correlated double sampling (CDS) column readout circuitry;

Figure 2 illustrates a column readout circuitry in accordance with the present invention.

Figure 3 illustrates the control signals for the column readout circuitry; and

Figures 4 to 7 schematically exemplify the four steps for the readout process.

Detailed Description of the Invention

A basic correlated double sampling (CDS) column readout circuitry 100 is shown in figure 1. Circuitry 100 includes an operational amplifier 101, capacitors 105 and 107 and transistors 102, 107, 109 and 110. The column bit-line is connected via line 120 to the source of transistor 102. From this bit-line the circuit 100 will successively sample a first active pixel charge V_A and then a reset pixel charge V_B in the following manner.

During a first period, a high value signal $Ø_A$ is applied to the gates of transistors 102, 106, 110 rendering them conductive. Transistor 109 is non-conducting due to a low signal on its gate. During this period, the feedback capacitor 107 is charged to the op amp 101 offset voltage V_{OS1}, and the input capacitor 105 is charged to the difference between the input pixel voltage V_A and the reference voltage V_{REF} on line 115 minus the op amp offset voltage V_{OS1}. Thus the charge Q_1 on capacitor 105 is such that:

$$Q_1 = [V_A - (V_{REF} - V_{OS1})]\, C_1$$

During a second period, transistors 106 and 110 are placed in non-conducting mode, and transistors 102 and 109 are placed in conducting mode by applying a high value signal $Ø_B$ to the gates of transistors 102 and 109. This places the op-amp 101 in its charge feedback amplification configuration. Concurrently, V_B is applied on line 120. Provided the capacitors 105 and 107 are matched in capacitance, the offset voltage V_{OS1} stored on the feedback capacitor 107 compensates for the op amp voltage offset V_{OS2}, and the difference in input voltages is propagated to the output terminal 113 as V_O, where

$$V_O = V_{REF} + V_A - V_B.$$

However, if the capacitors 105 and 107 are mismatched the voltage differential (V_A - V_B) will be amplified and the stored op-amp offset voltage V_{OS1} will not cancel the amplified effects of the offset voltage V_{OS2} during the second sampling. This produces the column-wise FPN due to capacitor mismatching.

This problem is resolved in accordance with the present invention by column

readout circuitry 200, which is illustrated in figure 2 with corresponding clocking signals for the readout circuitry shown in figure 3. Figure 3 illustrates clocking signals $Ø_1$, $Ø_2$, $Ø_3$ and $Ø_4$. The combined clocking signals $Ø_1 + Ø_4$, $Ø_2 + Ø_3$, as well as $Ø_1 + Ø_3$ that are applied to transistors 210, 202 and 206 respectively are also shown. The sample signals V_{S1} and V_{S2} are also shown on figure 3. Circuitry 200 comprises several switching devices such as NMOS transistors 202, 203, 206, 209, 210 and 214 for controlling the flow of charge through the readout circuitry 200, two capacitor elements 205 and 207 for the storage of the charge readouts of the pixel, and an operational amplifier 201 for amplifying the eventual readout value. In the drawing and subsequent description, the values C_1 and C_2 of capacitors 205 and 207 respectively are not equal, due to differences that are inherent in the process of creating an integrated circuit, known in this case as process mismatch. It is the intention of the invention to effectively render these differences irrelevant by removing the reliance of the amplifier 201on the values of capacitors 205 and 207.

In the first or reset step of the readout, as illustrated in figure 4, the column readout circuitry 200 is reset by setting Ø1 to a high logic level on the gates of transistors 203, 206, and 210 placing them in a conducting state. All other transistors are left in a non-conducting state. This connects the reference voltage V_{REF} to the anode of the first capacitor element 205 and to the anode of the second capacitor 207. This step sets the charge on the capacitors 205 and 207 to the offset voltage V_{OS} of the operational amplifier 201 and the output V_O to the reference voltage V_{REF} less the offset voltage V_{OS}. To summarize:

$$V_{C1} = V_{OS} \qquad \textit{(Equation 1.1)}$$

$$V_{C2} = V_{OS} \qquad \textit{(Equation 1.2)}$$

$$V_O = V_{REF} - V_{OS} \qquad \textit{(Equation 1.3)}$$

The second step, as illustrated in figure 5 is to acquire the first sample signal V_{S1}. This is accomplished by setting $Ø_1$ back to a logic low level, and raising $Ø_2$ to a logic high level. When $Ø_2$ is applied to the gates of transistors 202 and 209, they are placed in a conductive state. All other transistors are in a non-conducting state. The line 220 is

connected, through the column line, to the pixel element, which has the first sample voltage V_{S1}.

The anode of the first capacitor 205 had been precharged to V_{REF}, with the introduction of V_{S1} onto this node, a charge difference has been created. Due to the law of conservation of charge, there can be no net change in charge between the two capacitors 205 and 207. In other words:

$$Q_1 + Q_2 = K \qquad \textit{(Equation 2.1)}$$

where Q is the charge associated with a capacitor,
ΔQ is the charge difference on a capacitor, and
K is a constant

Or,

$$\Delta Q_1 + \Delta Q_2 = 0$$

From the law of conservation of charge, the equations associated with the circuit can now be determined.

$$V_{C1} = V_{S1} - (V_{REF} - V_{OS}) \qquad \textit{(Equation 2.2)}$$

From the law of conservation of charge,

$$\Delta V_{C1} = -(V_{REF} - V_{S1})$$

$$\Delta Q_1 = -(V_{REF} - V_{S1}) \times C_1$$

Subsequently,

$$\Delta Q_2 = -\Delta Q1$$

$$\Delta Q_2 = +(V_{REF} - V_{S1}) \times C_1$$

And,

$$V_{C2} = V_{C2OLD} + \Delta Q_2/C_2$$

Therefore,

$$V_{C2} = V_{OS} + (C_1/C_2) \times (V_{REF} - V_{S1}) \qquad \textit{(Equation 2.3)}$$

As well, since,

$$V_{C2} = V_O - (V_{REF} - V_{OS})$$

It can be said that,

$$V_O = V_{REF} + (C_1/C_2) \times (V_{REF} - V_{S1}) \qquad \textit{(Equation 2.4)}$$

Essentially, the circuit has completed its first sample of the pixel data. This was accomplished by placing the first sample signal onto the first capacitor 205 and then transferring the captured first pixel data into the second capacitor 207. This allows circuit space on the first capacitor 205, with which to capture the second sample V_{S2} of pixel data.

The third step comprising the acquisition of the second sample signal V_{S2}, as illustrated in figure 6, is done by setting the $Ø_2$ signal back to a logic low level, and setting the $Ø_3$ signal to a high logic level. This places transistors 202 and 206 in a conducting state, and leaves all the other transistors in the circuit 200 in a non-conducting state.

This allows the second sample signal V_{S2} from line 220 to be placed on the anode of the first capacitor 205. The voltage across the capacitor 205 has the following value,

$$V_{C1} = V_{S2} - (V_{REF} - V_{OS}) \qquad \textit{(Equation 3.1)}$$

As well since the output of the op-amp 201 has now been tied to the inverting input 216 of the op-amp 201,

$$V_O = V_{REF} - V_{OS} \qquad \textit{(Equation 3.2)}$$

In addition, the second capacitor element 207 has had its anode disconnected from any influencing potential, and its cathode is maintained at the same voltage as the previous step, allowing it to maintain the charge of the previous step. So,

$$V_{C2} = V_{OS} + (C_1/C_2) \times (V_{REF} - V_{S1}) \qquad \textit{(Equation 3.3)}$$

Essentially, the first sample signal V_{S1} was captured and stored on the second capacitor 207. Then the second sample signal V_{S2} was captured and stored on the first capacitor element 205. This leaves only the step of evaluation of the two pixel-data values.

The fourth step concerning pixel-data evaluation, as illustrated in figure 7, is accomplished by setting $Ø_3$ back to a logic low level and bringing $Ø_4$ to a logic high level. The $Ø_4$ clock signal controls transistors 214 and 210, setting $Ø_4$ high on the gates of transistors 214 and 210 places transistors 214 and 210 in a conducting state, while leaving all other transistors in a non-conducting state.

The anode of capacitor 207 is now connected to V_{REF}, and its cathode is now connected to $(V_{REF} - V_{OS})$, due to the virtual short circuit between the inputs of the op-amp 201. This establishes a charge on capacitor 207 of:

$$Q_2 = V_{REF} - (V_{REF} - V_{OS}) \times C_2$$

Therefore,

$$V_{C2} = V_{OS} \qquad \textit{(Equation 4.1)}$$

According to the law of conservation of charge,

$$\Delta Q_1 + \Delta Q_2 = 0$$

Therefore,

$$\Delta V_{C2} = V_{C2NEW} - V_{C2OLD}$$

$$\Delta V_{C2} = V_{OS} - [(C_1/C_2) \times (V_{REF} - V_{S1}) + V_{OS}]$$

$$= - (C_1/C_2) \times (V_{REF} - V_{S1})$$

$$\Delta Q_2 = C_2 \times \Delta V_{C2}$$

$$= - C_1 \times (V_{REF} - V_{S1})$$

And since,

$$\Delta Q_1 = -\Delta Q_2$$

Then,

$$\Delta V_{C1} = \Delta Q_1/C_1$$
$$= V_{REF} - V_{S1}$$
$$V_{C1} = V_{C1OLD} + \Delta V_{C1}$$
$$= (V_{S2} - (V_{REF} - V_{OS})) + (V_{REF} - V_{S1})$$
$$V_{C1} = V_{S2} - V_{S1} + V_{OS} \qquad \textit{(Equation 4.2)}$$

It can also be said that,

$$V_{C1} = V_O - (V_{REF} - V_{OS})$$

Therefore,

$$V_O = V_{C1} + (V_{REF} - V_{OS})$$

So, it can be determined that,

$$V_O = V_{S2} - V_{S1} + V_{REF} \qquad \textit{(Equation 4.3)}$$

In terms of what has occurred, the charge stored in the second capacitor 207 has been transferred back to the first capacitor 205 and left an evaluation at the output V_O of the circuit 200. An evaluation that is independent of the values of the capacitors 205 and 207 used in the amplifier, thus effectively eliminating the noise associated with the capacitors 205 and 207 due to process mismatch. In addition, the present invention is equally applicable even if the difference between the capacitors 205 and 207 is small or nonexistent.

Thus in the above details has been described a unique and useful column readout circuit for a CMOS imager. However, the invention is not necessarily limited to CMOS imagers, the invention could be used in any circumstance where an evaluation of two electrical signals must be performed without noise from the readout circuitry.

While the invention has been described according to what is presently considered to be the most practical and preferred embodiments, it must be understood that the invention is not limited to the disclosed embodiments. Those ordinarily skilled in the art will understand that various modifications and equivalent structures and functions may be made without departing from the spirit and scope of the invention as defined in the claims. Therefore, the invention as defined in the claims must be accorded the broadest possible interpretation so as to encompass all such modifications and equivalent structures and functions.